Improved Bounds on the Space Complexity of Circuit Evaluation

Yakov Shalunov

University of Chicago

Computational Complexity Conference · Lisbon · 2026

Williams' simulation theorem

$$\mathsf{TIME}[t] \subseteq \mathsf{SPACE}\left[\sqrt{t \log t}\right]$$

Hopcroft–Paul–Valiant

$O(t/\log t)$

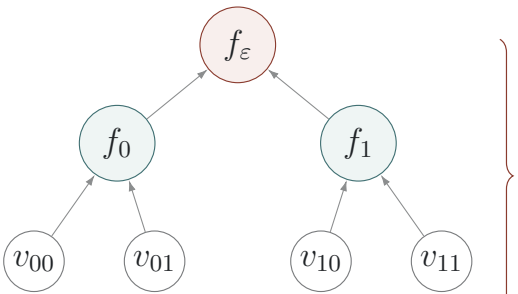
1977

Williams

$O(\sqrt{t \log t})$

2025

Tree evaluation



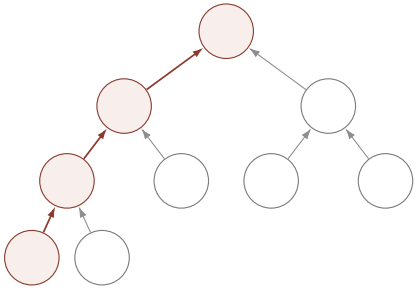
$$v_\ell \in \{0,1\}^b$$

$$v_\ell = f_\ell(v_{\ell 0}, v_{\ell 1})$$

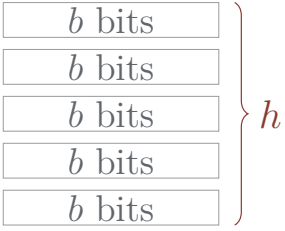
$$f_\ell : \{0,1\}^{2b} \downarrow \{0,1\}^b$$

Goal: evaluate the root, v_ε

Naive recursive evaluation

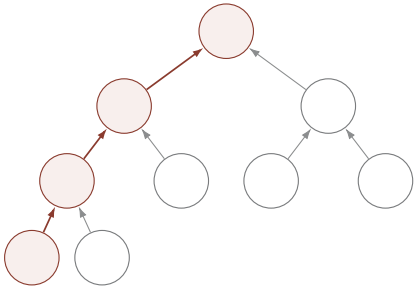


one b-bit value per level

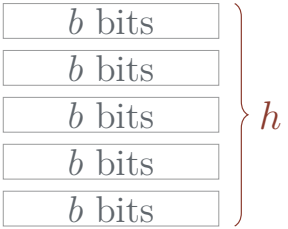


$\Theta(hb)$ space

Naive recursive evaluation



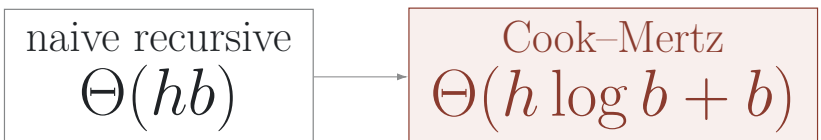
one b-bit value per level



$\Theta(hb)$ space

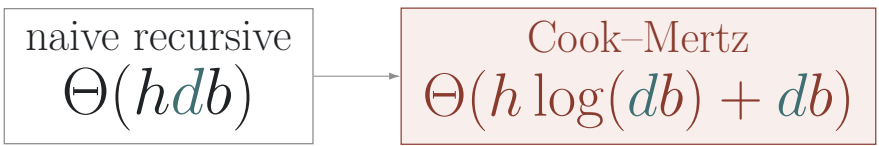
$$n = \widetilde{\Theta}(2^h \cdot 2^{2b}) \quad \text{so} \quad \Theta(hb) = \Theta(\log^2 n)$$

Cook–Mertz tree evaluation



The b-bit cost is paid once.

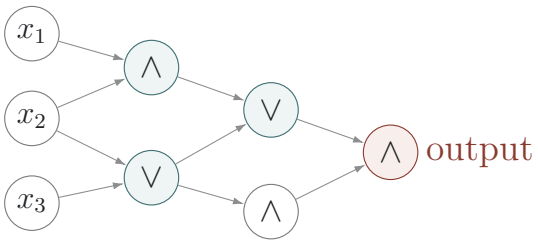
Tree evaluation with arity d



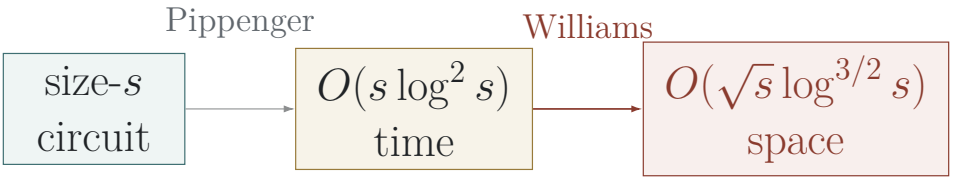
The db-bit cost is paid once.

Circuit evaluation problem

How much workspace is needed to evaluate a size-s circuit?



Inherited bound



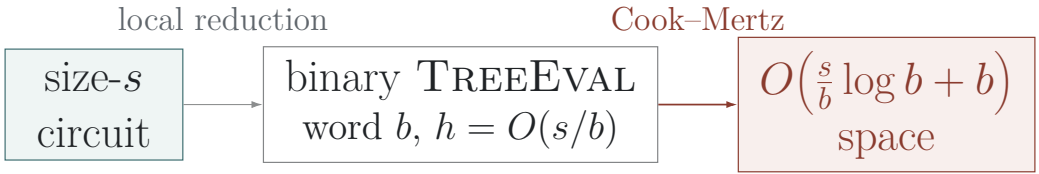
Can we do better using a direct reduction?

Main theorem

A size-s circuit can be evaluated in

$$O\left(\sqrt{s \log s}\right) \quad \text{space.}$$

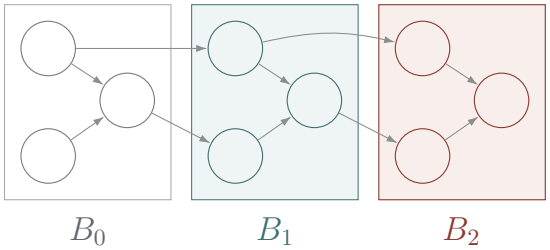
Reduction to tree evaluation



choose $b \sim \sqrt{s \log s}$

$O(\sqrt{s \log s})$ space

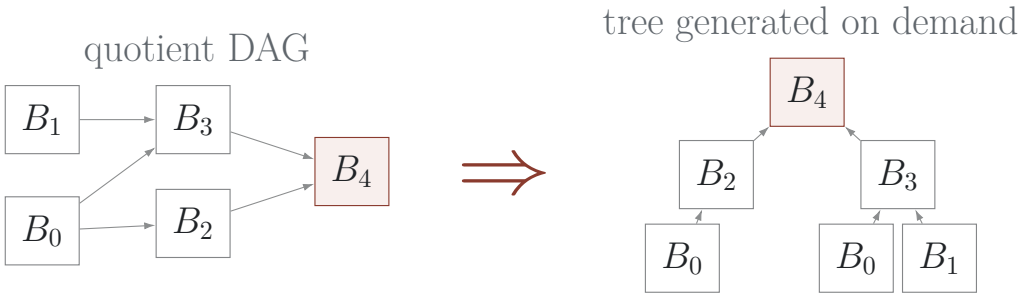
Naive block partition



Consecutive blocks of b gates.

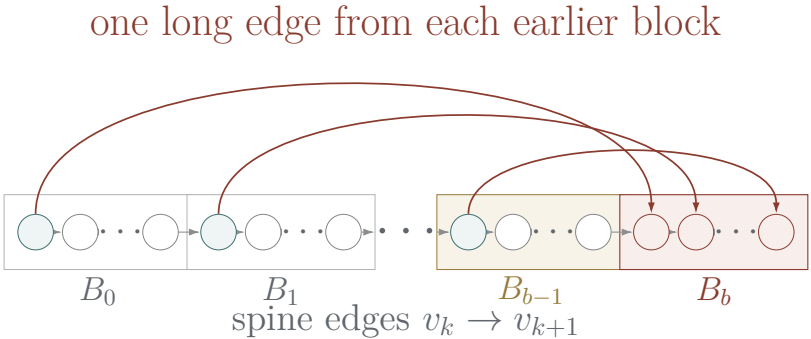
Each block evaluates to a b-bit value.

Unfold the quotient



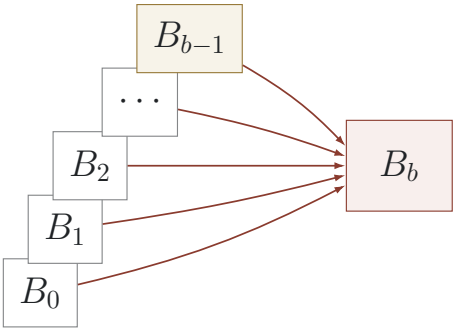
Exponential size is harmless; height is unchanged.

The in-degree obstruction



Every gate has in-degree at most 2.

The in-degree obstruction



$$\text{arity } d = \Theta(b)$$

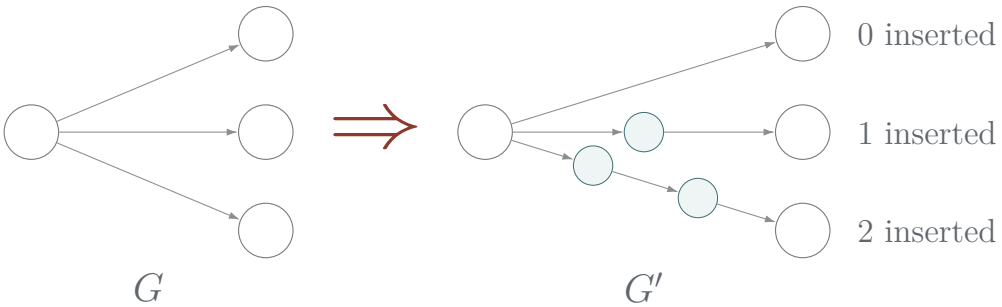
$$\Downarrow$$

$$O\left(\frac{s}{b}\log(b^2) + b^2\right)$$

choose $b \approx s^{1/3}$

$$\widetilde{O}(s^{2/3}) \text{ space}$$

Ingredient: subdivision



Each edge is replaced by a path.

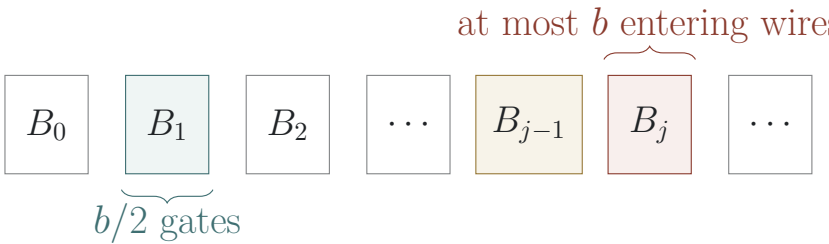
Low-in-degree partition lemma

LEMMA. For a graph G, there are some subdivision G' and partition P satisfying

$$|B| \leq b \qquad \Delta^-(G'/P) \leq 2$$

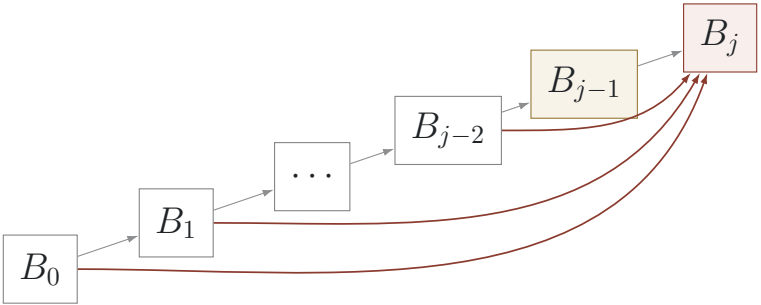
$$\text{height}(G'/P) = O(s/b)$$

Initial blocks



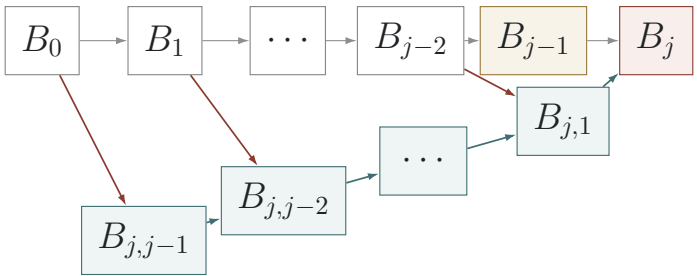
Use consecutive blocks of $b/2$ gates.

Long wires into B_j



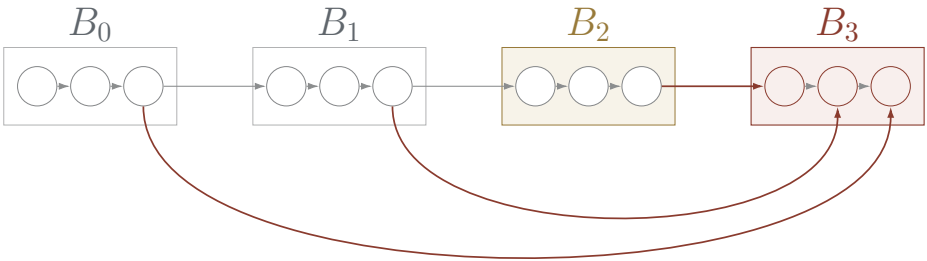
Build one cable for each initial block.

The cable for B_j



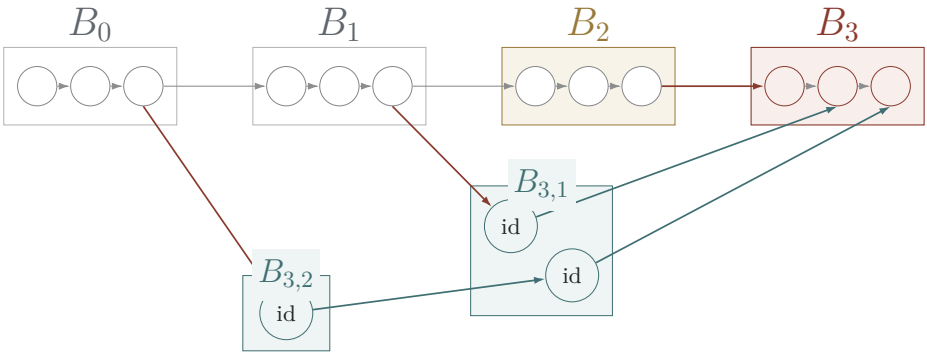
Identity vertices at wire–layer crossings.

Concrete example



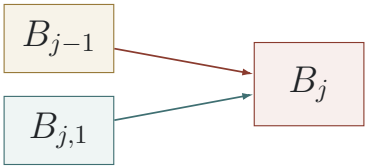
All three earlier blocks enter B_3.

Concrete example

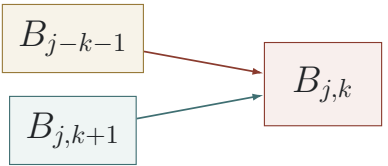


At most two predecessors per block.

Verification



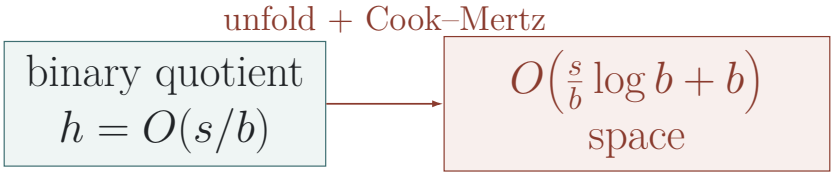
initial block



cable block

$|B_{j,k}| \leq b$ $\Delta^- \leq 2$ $h = O(s/b)$

Completing the reduction



With $b \sim \sqrt{s \log s}$,

$$O\left(\sqrt{s \log s}\right) \quad \text{space.}$$

Thank you

Open questions

Can we beat $\mathrm{depth}(C)$ when $\mathrm{depth}(C) < o(\sqrt{s})$?

Can we remove the $\log s$ factor without improving the general tree-evaluation algorithm?

Formal reduction

For every $b \in [2, s]$, a topologically sorted size-s circuit is locally reducible to a TreeEval instance with

$$d = 2, \qquad h = O(s/b), \qquad b\text{-bit words.}$$

Given a tree address u and $x, y \in \{0,1\}^b$, the node function $f_u(x, y)$ is computable in $O(b + \log s)$ space.

General tradeoff

For maximum in-degree d and target in-degree $d' \in \{2, \ldots, d+1\}$,

$$|B| \leq b, \qquad \Delta^-(G'/P) \leq d',$$

$$\text{height}(G'/P) = O\left(\frac{d}{d'-1}\frac{s}{b}\right).$$

Use $d'-1$ parallel cables of bandwidth b; rounding affects only constants.

Two consequences

Nonuniformly

A size-s circuit has a branching program of size

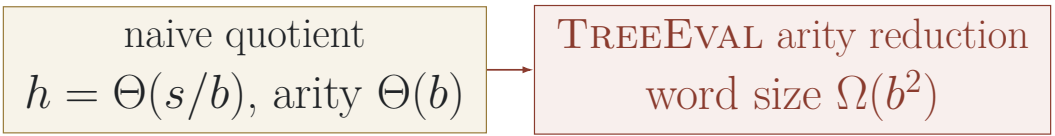
$2^{O(\sqrt{s \log s})}$.

Returning to time

Standard time-to-circuit simulation gives

$\mathsf{TIME}[t] \subseteq \mathsf{SPACE}[\sqrt{t} \log t]$.

Why arity comes first



The cables exploit the original DAG structure before it is lost.